What is claimed is:

1. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
at least two of the following system blocks:
an Error Checking & Correction Circuit (ECC);
a Checkerboard Memory Array containing sub arrays;
a Write Controller;
a Charge Pump;
a Vread Generator;
an Oscillator;
a Band Gap Reference Generator; and
a Page Register/Fault Memory.

2. The invention of Claim 1, further comprising a third system block.

3. The invention of Claim 1, wherein one of the system blocks is the Vread Generator.

4. The invention of Claim 3, wherein the Vread Generator provides a voltage to which a selected word line is driven during a read operation.

5. The invention of Claim 4, wherein two control transistors per group of memory sub arrays are spatially distributed throughout the die to achieve reduced voltage drop along reference node Vread.

6. The invention of Claim 1, wherein one of the system blocks is the write controller, and wherein groups of selected sub arrays are connected together by bidirectional data lines and are connected to the write controller.

7. The invention of Claim 6, wherein selected cells are in selected sub arrays, each of which has a coordinated row decoder for locating the selected cells.

8. The invention of Claim 1, wherein one of the system blocks is the write controller, and further comprising a fault memory and a logic block, wherein entries in the fault memory are determined by the write controller during the write operation and read by the logic block to activate a write operation to a redundant row.

9. The invention of Claim 6, wherein the connection between the groups of sub arrays and the write controller includes data lines and control lines, said lines which are at least partially formed on a level of wiring at or near a top surface of the memory array.

10. The invention of Claim 9 wherein the data and control lines are substantially parallel to memory array lines used for sensing data in memory cells.

11. The invention of Claim 6, wherein the selected sub arrays contain user data cells, ECC data cells and cells containing redundancy control bits.

12. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array;
a smart write controller; and
an oscillator.

13. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array;
a smart write controller;
a collection of memory sub arrays; and
a bi-directional connection between the memory sub arrays and the smart write controller.

14. The invention of Claim 13, wherein, during a write operation, information is transferred bi-directionally.

15. The invention of Claim 14, wherein data is transferred to the sub array for programming cells in the sub array and programming success is indicated to the smart write controller on the bi-directional connection.

16. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and.
a Checkerboard Memory Array containing sub arrays

17. The invention of Claim 16, wherein wiring above memory cells connects the subarrays to a write controller.

18. The invention of Claim 16, wherein a bi-directional connection is used between the memory subarrays and a smart write controller.

19. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
a set of selected sub arrays containing the combination of user data, ECC data, and reducndancy control bits.

20. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array;
a Checkerboard Memory Array containing sub arrays; and
ECC.

21. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array;
ECC; and

smart write.

22. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array;
ECC; and
on-the-fly redundancy.

23. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
a Vread generator with distributed output.

24. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
Smart write plus dummy bit lines.

25. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
data from a page register is distributed in a corresponding physical row in each of the sub arrays.

26. The invention of Claim 25, wherein each row contains the page register data, as well as ECC data and redundancy control bits.

27. A chip-level architecture comprising:
a monolithic three-dimensional write-once memory array; and
a die organization having two control (driver) transistors per memory line, plus row decoders and bias circuits that are shared amongst memory lines.

28. The invention of Claim 27 further comprising smart write.

29. A system or apparatus supported by any term, concept, feature, drawing, method, apparatus, system, etc. or portion thereof described in the above-listed documents, alone or in combination with any other term, concept, feature, drawing, method, apparatus, system, etc. or portion thereof described in the above-listed documents.

30. A method supported by any term, concept, feature, drawing, method, apparatus, system, etc. or portion thereof described in the above-listed documents, alone or in combination with any other term, concept, feature, drawing, method, apparatus, system, etc. or portion thereof described in the above-listed documents.